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**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number		10675721
Filing Date		2003-09-30
First Named Inventor	Levine et al.	
Art Unit	2191	
Examiner Name	Vo, Ted T.	
Attorney Docket Number	AUS920030483US1	

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Examiner Initial*	Cite No	Patent Number	Kind Code ¹	Issue Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear
TIV	1	6542985		2003-04-01	Johnson et al.	
TIV	2	4316245		1982-02-16	Luu et al.	
TIV	3	7181723		2007-02-20	Luk et al.	
TIV	4	6961925		2005-11-01	Callahan, II et al.	
TIV	5	5950003		1999-09-30	Kaneshiro et al.	
TIV	6	5212794		1993-05-18	Pettis et al.	
TIV	7	5659679		1997-08-19	Alpert et al.	
TIV	8	6006033		1999-12-21	Heisch	

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TTU ✓	9	6119075		2000-09-12	Dean et al.	
TTU ✓	10	6189141	B1	2001-02-13	Benitez et al.	
TTU ✓	11	6237141	B1	2001-05-22	Holzle et al.	
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TTU ✓	14	6631514	B1	2003-10-07	Le	
TTU ✓	15	5794028		1998-08-11	Tran	
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TTU ✓	19	5752062		1998-05-12	Gover et al.	

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TTU	20	6446029	B1	2002-09-03	Davidson et al.	
TTU	21	5970439		1999-10-19	Levine et al.	

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TU	1	RAMIREZ et al., "The Effect of Code Reordering on Branch Prediction", Proceedings of the International Conference on Parallel Architectures and Compilation Techniques, October 2000, pp. 189-198.	<input type="checkbox"/>
	2	YANG et al., "Improving Performance by Branch Reordering", Proceedings of the ACM SIGPLAN 1998 Conference on Programming Language Design and Implementation, Montreal Canada, 1998, pp. 130-144. <i>location only</i>	<input type="checkbox"/>
TU	3	CONTE et al., "Accurate and Practical Profile-Driven Compilation Using the Profile Buffer", Proceedings of the 29th Annual ACM/IEEE International Symposium on Microarchitecture, Paris, France, 1996, pp. 36-45.	<input type="checkbox"/>
TU	4	CONTE et al., "Using Branch Handling Hardware to Support Profile-Driven Optimization", Proceedings of the 27th Annual International Symposium on Microarchitecture, San Jose CA, 1994, pp. 12-21.	<input type="checkbox"/>
TU	5	FISHER, "Trace Scheduling: A Technique for Global Microcode Compaction", IEEE Transactions on Computers, Vol. C30, No. 7, July 1981, pp. 478-490.	<input type="checkbox"/>
TU	6	CHANG et al., "Using Profile Information to Assist Classic Code Optimizations", Software Pract. Exper. 21, December 1991, pp. 1301-1321.	<input type="checkbox"/>
TU	7	SCHMIDT et al., "Profile-Directed Restructuring of Operating System Code", IBM Systems Journal, 1998, Vol. 37, No. 2, pp. 270-297.	<input type="checkbox"/>
TU	8	AHO et al., "Compilers: Principles, Techniques, and Tools", Addison-Wesley, 1988, pp. 488-497.	<input type="checkbox"/>

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TTU✓	9	6256771	B1	2001-07-03	O'Neil et al.	
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TTU	4	20030135719	A1	2003-07-17	DeWitt, Jr. et al.	
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